CLAIMS

1. An output driver impedance controller that controls pull-down impedance of at least one output based on a reference value, comprising:

a programmable reference impedance generator that develops a reference impedance controlled by a reference impedance control input;

at least one output driver, each including a programmable output impedance generator coupled to a corresponding output and controlled by an output impedance control input; and

an impedance matching controller that continually adjusts said reference impedance control input to match said reference impedance with the reference value within a predetermined tolerance and that generates said output impedance control input based on said reference impedance control input.

2. The output driver impedance controller of claim 1, wherein said programmable reference impedance generator and each of said at least one programmable output impedance generator comprises a binary array of matched impedance devices.

3. The output driver impedance controller of claim 2, wherein said binary array of matched impedance devices comprises matched N-channel devices.

4. The output driver impedance controller of claim 1, wherein said impedance matching controller comprises:

a voltage sensor that senses a voltage difference between a reference voltage based on an input bus voltage and a voltage of said programmable reference impedance generator and that asserts an error signal indicative thereof; and

impedance control logic that adjusts said reference impedance control input based on said error signal.

5. The output driver impedance controller of claim 4, wherein the reference value comprises a reference resistor, and wherein said input bus voltage is applied across said reference resistor and said programmable reference impedance generator coupled in series.

6. The output driver impedance controller of claim 4, wherein said impedance control logic receives a clock signal and increments or decrements said reference impedance control input during selected cycles of said clock signal.

7. The output driver impedance controller of claim 1, further comprising bias adjustment logic that combines a bias amount with said reference impedance control input to provide said output impedance control input.

8. The output driver impedance controller of claim 7, further comprising output bias logic that is programmed to provide said bias amount.

9. The output driver impedance controller of claim 1, wherein said impedance matching controller comprises:

a first controller for coupling to an external reference resistor that provides a first reference value; and

a second controller including an internal reference resistor that provides a second reference value.

10. The output driver impedance controller of claim 9, wherein said first controller includes detection logic that monitors said reference impedance control input to determine whether said first reference value is coupled and that enables said second controller if said first reference value is not coupled.

11. The output driver impedance controller of claim 1, wherein each said at least one output driver includes output enable logic.

12. An integrated circuit (IC), comprising:

a plurality of pins including a first reference pin for receiving a reference voltage and at least one output pin;

at least one output driver, each including a programmable output impedance generator controlled by an output impedance control input and coupled to drive a corresponding one of said at least one output pin; and

impedance matching logic, comprising:

a programmable reference impedance generator controlled by a reference impedance control input;

comparator logic that continually adjusts said reference impedance control input to equalize values of a reference resistor coupled to said first reference pin and said programmable reference impedance generator within a predetermined tolerance; and

output logic that controls said output impedance control input based on said reference impedance control input.

13. The IC of claim 12, wherein said reference voltage is applied across a series coupling of said reference resistor and said programmable reference impedance generator and wherein said comparator logic attempts to equalize voltages within a predetermined voltage tolerance.

14. The IC of claim 12, further comprising a second reference pin coupled to said programmable reference impedance generator and for coupling to one end of said reference resistor comprising an external reference resistor having its other end coupled to said first reference pin.

15. The IC of claim 14, wherein said impedance matching logic comprises:

an internal reference resistor having one end coupled to said first reference pin and a second end;

said programmable reference impedance generator including a first programmable reference impedance generator controlled by a first reference impedance control input and coupled to said second reference pin and a second programmable reference impedance generator controlled by a second reference impedance control input and coupled to said second end of said internal reference resistor;

said comparator logic including first comparator logic that adjusts said first reference impedance control input in an attempt to equalize voltages of said external reference resistor and of said first programmable reference impedance generator within a first tolerance, and second comparator logic that adjusts said second reference impedance control input in an attempt to equalize voltages of said internal reference resistor and of said second programmable reference impedance generator within a second tolerance;

detection logic that monitors said first reference impedance control input for detecting presence of said external reference resistor and providing an enable signal indicative thereof; and

said output logic selecting one of said first and second reference impedance control inputs based on said enable signal for providing said output impedance control input.

16. The IC of claim 15, further comprising:

output bias logic that provides an adjustment value; and

said output logic comprising bias adjustment logic that combines said reference impedance control input with said adjustment value to provide said output impedance control input.

17. The IC of claim 16, wherein said output bias logic comprises a plurality of fuses.

18. The IC of claim 12, wherein said programmable reference impedance generator and each said programmable output impedance generator comprises a binary array of matched N-channel impedance devices.

19. The IC of claim 12, wherein said comparator logic comprises:

a voltage sensor, coupled to said first reference pin and to said programmable reference impedance generator, that detects voltages across said reference resistor and said programmable reference impedance generator and that asserts an error signal indicative thereof; and

impedance control logic that adjusts said reference impedance control input based on said error signal.

20. The IC of claim 19, said reference impedance control input comprising a digital value, wherein said impedance control logic receives a clock signal and increments or decrements said reference impedance control input in response to selected cycles of said clock signal.

21. A method of controlling pull-down impedance of at least one output driver, comprising:

applying a reference voltage to a reference resistor and a reference impedance generator having a reference impedance input;

periodically adjusting the reference impedance input to equalize impedance of the reference impedance generator with the reference resistor within a predetermined tolerance; and

controlling an output impedance input of at least one output impedance generator based on the reference impedance input, each output impedance generator coupled to a corresponding output driver.

22. The method of claim 21, further comprising:

sensing voltage at a common junction of the reference impedance generator and the reference resistor coupled in series with the reference voltage; and

said periodically adjusting comprising comparing the voltage at the common junction with one-half of the reference voltage.

23. The method of claim 21, further comprising:

providing an internal reference resistor;

detecting an externally-coupled reference resistor and providing an enable signal indicative thereof; and

selecting between the internal and external reference resistors based on the enable signal.

24. The method of claim 21, wherein said periodically adjusting the reference impedance input comprises incrementing or decrementing a digital value during selected cycles of a clock signal.

25. The method of claim 21, further comprising:

programming a bias adjust value; and

said controlling an output impedance input comprising combining the bias adjust value with the reference impedance input.

26. The method of claim 21, further comprising enabling or disabling each output driver based on an output enable signal.

27. The method of claim 21, further comprising:

activating selected ones of a binary array of matched impedance devices of the reference impedance generator based on the reference impedance input; and

activating selected ones of a binary array of matched impedance devices of each output impedance generator based on the output impedance input.